IN THE CLAIMS:

Kindly amend the claims as follows:

1. (Original) A method for generating a Cyclic Redundancy Check (CRC) in a system comprising the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero,

wherein the step of programming is based on a pre-selected polynomial key word.

2. (Currently Amended) ~~The method as recited in Claim 1,~~ A method for generating a Cyclic Redundancy Check (CRC) in a system, comprising the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero,

wherein the step of programming is based on a pre-selected polynomial key word, and

wherein the step of programming comprises:

programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on the pre-selected polynomial key word;

the first set of selection inputs is associated with:

selecting corresponding input from each of the logic gates; and

a shift logic that is associated with the plurality of registers.

3. (Currently Amended) ~~The method as recited in Claim 1,~~ A method for generating a Cyclic Redundancy Check (CRC) in a system, comprising the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero,

wherein the step of programming is based on a pre-selected polynomial key word, and

wherein the step of programming comprises:

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each of the logic gates;

the second set of selection inputs is associated with the selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial key word.

4. (Original) The method as recited in Claim 1, further comprising:

using a first set of multiplexers in conjunction with a first set of selection inputs for selecting at least one input for shifting data to a next shift register of the plurality of registers,

wherein the at least one input is a member of a set of inputs that includes an output from an adjacent logic gate and a straight shift input from an adjacent register of the plurality of registers.

5. (Original) The method as recited in Claim 1, further comprising:

using a second set of multiplexers in conjunction with a second set of selection inputs for selecting at least one input to a corresponding logic gate,

wherein the at least one input is a member of a set of inputs that includes a primary input and a feedback input.

6. (Original) The method as recited in Claim 1, further comprising:

using a second set of multiplexers in conjunction with a second set of selection inputs for selecting a final output from among output from the plurality of registers.

7. (Original) The method as recited in Claim 1, wherein the plurality of registers are shift registers.

8. (Original) A method for generating a Cyclic Redundancy Check (CRC) generator in a system comprising the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection inputs is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

9. (Original) The method as recited in Claim 8, further comprising:

using a first set of multiplexers in conjunction with the first set of selection inputs for selecting at least one input for shifting to a next register of the plurality of registers,

wherein the at least one input is a member of a set of inputs that includes an output from an adjacent logic gate and a straight shift from an adjacent register of the plurality of registers.

10. (Original) The method as recited in Claim 8, further comprising:

using a second set of multiplexers in conjunction with the second set of selection inputs for selecting at least one input to a corresponding logic gate,

wherein the at least one input is a member of a set of inputs that includes a primary input and a feedback input.

11. (Original) The method as recited in Claim 8, further comprising:

using a second set of multiplexers in conjunction with the second set of selection inputs for selecting the final output from among output from the plurality of registers.

12. (Original) The method as recited in Claim 8, wherein the plurality of registers are shift registers.

13. (Original) A computer-readable medium carrying one or more sequences of instructions for generating a Cyclic Redundancy Check (CRC) generator in a system, which instructions, when executed by one or more processors, cause the one or more processors to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero,

wherein the step of programming is based on a pre-selected polynomial key word.

14. (Original) A computer-readable medium carrying one or more sequences of instructions for generating a Cyclic Redundancy Check (CRC) generator in a system, which

instructions, when executed by one or more processors, cause the one or more processors to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection inputs is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

15. (Original) An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

means for creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

means for programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero,

wherein the step of programming is based on a pre-selected polynomial key word.

16. (Original) An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

means for creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

means for programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection in puts is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

means for programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

means for the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

17. (Original) An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

a processor;

one or more stored sequences of instructions which, when executed by the processor, cause the processor to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero,

wherein the step of programming is based on a pre-selected polynomial key word.

18. (Original) An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

a processor;

one or more stored sequences of instructions which, when executed by the processor, cause the processor to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a first set of selection inputs wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection inputs is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among out put from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

19. (Currently Amended) A cyclic redundancy check (CRC) generator for generating CRC codes, comprising:

a first set of N storage elements,

wherein a first selection signal is configured to select a subset of the first set of N storage elements, and

wherein each storage element of the subset of the first set of N storage elements corresponds to a term of a pre-selected CRC polynomial keyword; and

M logic circuits,

wherein an input of each of the M logic circuits is in communication with an output of a corresponding one of the first set of N storage elements, and

wherein a second selection signal is configured to select an output of one storage element of the subset of the first set of N storage elements corresponding to a length of the pre-selected CRC polynomial keyword.

20. (Previously Presented) The CRC generator of claim 19, wherein each storage element of the first set of N storage elements corresponds to a term of an Nth-order CRC polynomial keyword, and

wherein the length of the pre-selected CRC polynomial keyword is at most N.

21. (Previously Presented) The CRC generator of claim 19, comprising:

a first plurality of selector circuits,

wherein each selector circuit of the first plurality of selector circuits is configured to output one of an output of a corresponding one of the M logic circuits and an output of a corresponding one of the first set of N storage elements, and

wherein each selector circuit of the first plurality of selector circuits is configured to receive the first selection signal based upon the pre-selected CRC polynomial keyword.

22. (Previously Presented) The CRC generator of claim 21, comprising:

a second set of N storage elements,

wherein each storage element of the second set of N storage elements is in communication with a corresponding one of the first set of N storage elements, and

wherein each storage element of the second set of N storage elements is configured to provide the first selection signal to the corresponding one of the first set of N storage elements based upon the pre-selected CRC polynomial keyword.

23. (Previously Presented) The CRC generator of claim 21, comprising:

a second plurality of selector circuits,

wherein each selector circuit of the second plurality of selector circuits is configured to output one of an output of a first subset of the first set of N storage elements and an output of a second subset of the first set of N storage elements, and

wherein one of the second plurality of selector circuits receives the second selection signal to select the output of the first subset of the first set of N storage elements for output.

24. (Previously Presented) The CRC generator of claim 23, comprising:

a third set of selector circuits,

wherein the output of each selector circuit of the third set of selector circuits is in communication with an input of a corresponding one of the M logic circuits,

wherein each selector circuit of the third set of selector circuits is configured to output one of an output of a corresponding one of the second set of selector circuits and an input signal, and

wherein one of the third plurality of selector circuits receives the second selection signal to select the input signal for output.

25. (Previously Presented) The CRC generator of claim 24, wherein each selector circuit comprises a multiplexer.

26. (Previously Presented) The CRC generator of claim 19, comprising:

an output selector circuit,

wherein inputs of the output selector circuit are in communication with outputs of each storage element of the first set of N storage elements, and

wherein the output selector circuit is configured to receive the second selection signal to select the output of the one storage element of the subset of the first set of N storage elements as the output of the CRC generator for the pre-selected CRC polynomial keyword.

27. (Previously Presented) The CRC generator of claim 26, wherein the output selector circuit comprises a multiplexer.

28. (Previously Presented) The CRC generator of claim 19, wherein an input of one of the M logic circuits is in communication with an input signal.

29. (Previously Presented) The CRC generator of claim 19, wherein each storage element of the first set of N storage elements comprises one of a shift register and a buffer.

30. (Previously Presented) The CRC generator of claim 19, wherein each of the M logic circuits comprises an XOR gate.

31. (Currently Amended) A cyclic redundancy check (CRC) generator for generating CRC codes, comprising:

a first set of N means for storing data,

wherein a first selection signal is configured to select a subset of the first set of N data storing means, and

wherein each data storing means of the subset of the first set of N data storing means corresponds to a term of a pre-selected CRC polynomial keyword; and

M logic circuit means,

wherein an input of each of the M logic circuit means is in communication with an output of a corresponding one of the first set of N data storing means, and

wherein a second selection signal is configured to select an output of one data storing means of the subset of the first set of data storing means corresponding to a length of the pre-selected CRC polynomial keyword.

32. (Previously Presented) The CRC generator of claim 31, wherein each data storing means of the first set of N data storing means corresponds to a term of an Nth-order CRC polynomial keyword, and

wherein the length of the pre-selected CRC polynomial keyword is at most N.

33. (Previously Presented) The CRC generator of claim 31, comprising:

a first plurality of means for signal selecting,

wherein each signal selecting means of the first plurality of signal selecting means is configured to output one of an output of a corresponding one of the M logic circuit means and an output of a corresponding one of the first set of N data storing means, and

wherein each signal selecting means of the first plurality of signal selecting means is configured to receive the first selection signal based upon the pre-selected CRC polynomial keyword.

34. (Previously Presented) The CRC generator of claim 33, comprising:

a second set of N means for storing data,

wherein each data storing means of the second set of N data storing means is in communication with a corresponding one of the first set of N data storing means, and

wherein each data storing means of the second set of N data storing means is configured to provide the first selection signal to the corresponding one of the first set of N data storing means based upon the pre-selected CRC polynomial keyword.

35. (Previously Presented) The CRC generator of claim 33, comprising:

a second plurality of means for signal selecting,

wherein each signal selecting means of the second plurality of signal selecting means is configured to output one of an output of a first subset of the first set of N data storing means and an output of a second subset of the first set of N data storing means, and

wherein one of the second plurality of signal selecting means receives the second selection signal to select the output of the first subset of the first set of N data storing means for output.

36. (Previously Presented) The CRC generator of claim 35, comprising:

a third set of means for signal selecting,

wherein the output of each signal selecting means of the third set of signal selecting means is in communication with an input of a corresponding one of the M logic circuit means,

wherein each signal selecting means of the third set of signal selecting means is configured to output one of an output of a corresponding one of the second set of signal selecting means and an input signal, and

wherein one of the third plurality of signal selecting means receives the second selection signal to select the input signal for output.

37. (Previously Presented) The CRC generator of claim 36, wherein each signal selecting means comprises a multiplexer means.

38. (Previously Presented) The CRC generator of claim 31, comprising:

an output means for signal selecting,

wherein inputs of the output signal selecting means are in communication with outputs of each data storing means of the first set of N data storing means, and

wherein the output signal selecting means is configured to receive the second selection signal to select the output of the one data storing means of the subset of the first set of N data storing means as the output of the CRC generator for the pre-selected CRC polynomial keyword.

39. (Previously Presented) The CRC generator of claim 38, wherein the output signal selecting means comprises a multiplexer means.

40. (Previously Presented) The CRC generator of claim 31, wherein an input of one of the M logic circuit means is in communication with an input signal.

41. (Previously Presented) The CRC generator of claim 31, wherein each data storing means of the first set of N data storing means comprises one of a means for shifting data and a means for buffering data.

42. (Previously Presented) The CRC generator of claim 31, wherein each of the M logic circuit means comprises an XOR gate means.

43. (Previously Presented) A method of generating cyclic redundancy check (CRC) codes, comprising the steps of:

a.) storing a first signal N times;

b.) logically combining each stored first signal with one of an input signal and a selected signal M times;

c.) selecting a subset of the N storing steps in response to a first selection signal, wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and

d.) selecting an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword, in response to a second selection signal.

44. (Previously Presented) The method of claim 43, wherein each storing step of the N storing steps corresponds to a term of an Nth-order CRC polynomial keyword, and wherein the length of the pre-selected CRC polynomial keyword is at most N.

45. (Previously Presented) The method of claim 44, comprising the step of:

e.) selecting one of an output of a corresponding one of the M logically combining steps and an output of a corresponding one of the N storing steps in response to the first selection signal.

46. (Previously Presented) The method of claim 45, comprising the step of:

f.) selecting one of an output of a first subset of the N storing steps and an output of a second subset of the N storing steps, in response to the second selection signal.

47. (Previously Presented) The method of claim 46, comprising the step of:

g.) selecting one of an output of step (f) and an input signal to form the selected signal, in response to the second selection signal.

48. (Previously Presented) The method of claim 43, comprising the step of:

e.) selecting the output of the one of the storing steps of the subset of N storing steps as the output of the pre-selected CRC polynomial keyword, in response to the second selection signal.

49. (Previously Presented) The method of claim 43, comprising the step of:

e.) receiving an input signal at one of the M logically combining steps.

50. (Previously Presented) The method of claim 43, wherein each of the N storing steps comprises the step of shifting the first signal.

51. (Previously Presented) The method of claim 43, wherein each of the M logically combining steps comprises the step of exclusive or'ing the respective stored first signal with a corresponding one of the input signal and the selected signal.

52. (Previously Presented) A computer program for generating cyclic redundancy check (CRC) codes, wherein the computer program performs the steps of:

a.) controlling storing of a first signal N times;

b.) logically combining each stored first signal with one of an input signal and a selected signal M times;

c.) providing a first selection signal to select a subset of the N storing steps, wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and

d.) providing a second selection signal to select an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword.

53. (Previously Presented) The computer program of claim 52, wherein each storing step of the N storing steps corresponds to a term of an Nth-order CRC polynomial keyword, and

wherein the length of the pre-selected CRC polynomial keyword is at most N.

54. (Previously Presented) The computer program of claim 53, wherein the computer program performs the step of:

e.) providing the first selection signal to select one of an output of a corresponding one of the M logically combining steps and an output of a corresponding one of the N storing steps.

55. (Previously Presented) The computer program of claim 54, wherein the computer program performs the step of:

f.) providing the second selection signal to select one of an output of a first subset of the N storing steps and an output of a second subset of the N storing steps.

56. (Previously Presented) The computer program of claim 55, comprising the step of:

g.) providing the second selection signal to select one of an output of step (f) and an input signal to form the selected signal.

57. (Previously Presented) The computer program of claim 52, wherein the computer program performs the step of:

e.) providing the second selection signal to select the output of the one of storing steps of the subset of the N storing steps as the output of the pre-selected CRC polynomial keyword.

58. (Previously Presented) The computer program of claim 52, wherein the computer program performs the step of:

e.) providing an input signal at one of the M logically combining steps.

59. (Previously Presented) The computer program of claim 52, wherein each of the N storing steps comprises the step of shifting the first signal.

60. (Previously Presented) The computer program of claim 52, wherein each of the M logically combining steps comprises the step of exclusive or'ing the respective stored first signal with a corresponding one of the input signal and the selected signal.

61. (Previously Presented) The CRC generator of claim 19, wherein M is equal to N.

62. (Previously Presented) The CRC generator of claim 22, wherein each storage element of the second set of N storage elements comprises one of a register and a buffer element.

63. (Previously Presented) The CRC generator of claim 31, wherein M is equal to N.

64. (Previously Presented) The CRC generator of claim 34, wherein each data storing means of the second set of N data storing means comprises one of a means for shifting data and a means for buffering data.

65. (Previously Presented) The method of claim 43, wherein M is equal to N.

66. (Previously Presented) The computer program of claim 52, wherein M is equal to N.

67. (Previously Presented) A cyclic redundancy check (CRC) generator for generating CRC codes, comprising:

N CRC subcircuits,

wherein each of the N CRC subcircuits comprises:

a storage element;

a logic circuit in communication with the storage element; and

a first selector circuit in communication with an output of the storage element and an output of the logic circuit,

wherein an input of a storage element of an nth one of the N CRC subcircuits is in communication with an output of a first selector circuit of an n-1th one of the N CRC subcircuits,

wherein a first selection signal is configured to select a subset of the N CRC subcircuits, and

wherein each storage element of the subset of the N CRC subcircuits corresponds to a term of a pre-selected CRC polynomial keyword;

M selector subcircuits,

wherein each of the M selector subcircuits comprises:

a second selector circuit,

wherein a first input of the second selector circuit of an mth one of the M selector subcircuits is in communication with an output of a second selector circuit of an m+1th one of the M selector subcircuits, and

wherein a second input of the second selector circuit of the mth one of the M selector subcircuits is in communication with an output of a first selector circuit of the nth one of the N CRC subcircuits; and

a third selector circuit,

wherein a first input of the third selector circuit of the mth one of the M selector subcircuits is in communication with an output of the second selector circuit of the mth one of the M selector subcircuits, and

wherein a second input of the third selector circuit of the mth one of the M selector subcircuits is in communication with an input signal,

wherein the second and third selector circuits of one of the M selector subcircuits receive a second selection signal to select the second input of the respective second and third selector circuits for output; and

an output selector circuit,

wherein inputs of the output selector circuit are in communication with outputs of each storage element of the N CRC subcircuits, and

wherein the output selector circuit receives the second selection signal to select the output of one storage element of the subset of the N CRC subcircuits corresponding to a length of the pre-selected CRC polynomial keyword.

68. (Previously Presented) The CRC generator of claim 67, wherein M is equal to N-1, and

wherein an output of an Nth CRC subcircuit is in communication with the first input of the second selector circuit of the Mth selector subcircuit.

69. (Previously Presented) The CRC generator of claim 67, wherein each storage element comprises one of a shift register and a buffer.

70. (Previously Presented) The CRC generator of claim 67, wherein each logic circuit comprises an XOR gate.

71. (Previously Presented) The CRC generator of claim 67, wherein each of the M selector subcircuits comprises a multiplexer subcircuit, and

wherein each of the first, second and third selector circuits comprises a multiplexer.

72. (Previously Presented) A cyclic redundancy check (CRC) generator for generating CRC codes, comprising:

N CRC subcircuit means,

wherein each of the N CRC subcircuit means comprises:

a means for storing data;

a logic circuit means in communication with the data storing means; and

a first means for signal selecting in communication with an output of the data storing means and an output of the logic circuit means,

wherein an input of a data storing means of an nth one of the N CRC subcircuit means is in communication with an output of a first signal selecting means of an n-1th one of the N CRC subcircuit means,

wherein a first selection signal is configured to select a subset of the N CRC subcircuit means, and

wherein each data storing means of the subset of the N CRC subcircuit means corresponds to a term of a pre-selected CRC polynomial keyword;

M selector subcircuit means,

wherein each of the M selector subcircuit means comprises:

a second means for signal selecting,

wherein a first input of the second signal selecting means of an mth one of the M selector subcircuit means is in communication with an output of a second signal selecting means of an m+1th one of the M selector subcircuit means, and

wherein a second input of the second signal selecting means of the mth one of the M selector subcircuit means is in communication with an output of a first signal selecting means of the nth one of the N CRC subcircuit means; and

a third means for signal selecting,

wherein a first input of the third signal selecting means of the mth one of the M selector subcircuit means is in communication with an output of the second signal selecting means of the mth one of the M selector subcircuit means, and

wherein a second input of the third signal selecting means of the mth one of the M selector subcircuit means is in communication with an input signal,

wherein the second and third signal selecting means of one of the M selector subcircuit means receive a second selection signal to select the second input of the respective second and third signal selecting means for output; and

an output means for signal selecting,

wherein inputs of the output signal selecting means are in communication with outputs of each data storing means of the N CRC subcircuit means, and

wherein the output signal selecting means receives the second selection signal to select the output of one data storing means of the subset of the N CRC subcircuit means corresponding to a length of the pre-selected CRC polynomial keyword.

73. (Previously Presented) The CRC generator of claim 72, wherein M is equal to N-1, and

wherein an output of an Nth CRC subcircuit means is in communication with the first input of the second signal selecting means of the Mth selector subcircuit means.

74. (Previously Presented) The CRC generator of claim 72, wherein each data storing means comprises one of a means for shifting data and a means for buffering data.

75. (Previously Presented) The CRC generator of claim 72, wherein each logic circuit means comprises an XOR gate means.

76. (Previously Presented) The CRC generator of claim 72, wherein each of the M selector subcircuit means comprises a multiplexer subcircuit means, and

wherein each of the first, second and third signal selecting means comprises a multiplexer means.

77. (Previously Presented) A method of generating cyclic redundancy check (CRC) codes, comprising the steps of:

a.) shifting a first signal N times,

b.) exclusive or'ing each shifted first signal with one of an input signal and a selected signal M times;

c.) selecting one of an output of a corresponding one of the M exclusive or'ing steps and an output of a corresponding one of the N storing steps, in response to a first selection signal,

wherein an input of an nth one of the N shifting steps is in communication with an output of an n-1th one of the N selecting steps of step (c);

d.) selecting, M times, one of an output of a first subset of the N storing steps and an output of a second subset of the N storing steps, in response to a second selection signal,

wherein a first input of an mth one of the selecting steps of step (d) is in communication with an output of an m+1th one of the selecting steps of step (d), and

wherein a second input of the mth one of the selecting steps of step (d) is in communication with an output of an nth one of the selecting steps of step (c);

e.) selecting, M times, one of an output of step (d) and an input signal to form the selected signal, in response to the second selection signal;

f.) selecting a subset of the N storing steps in response to the first selection signal,

wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and

g.) selecting an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword as the output of the pre-selected CRC polynomial keyword, in response to the second selection signal.

78. (Previously Presented) The method of claim 77, wherein M is equal to N-1, and

wherein an output of an Nth selecting step of step (c) is in communication with the first input of an Mth selecting step of step (d).

79. (Previously Presented) A computer program for generating cyclic redundancy check (CRC) codes, wherein the computer program performs the steps of:

a.) controlling shifting of a first signal N times,

b.) exclusive or'ing each shifted first signal with one of an input signal and a selected signal M times;

c.) providing a first selection signal to select one of an output of a corresponding one of the M exclusive or'ing steps and an output of a corresponding one of the N storing steps,

wherein an input of an nth one of the N shifting steps is in communication with an output of an n-1th one of the N selectings of step (c);

d.) providing a second selection signal to select, M times, one of an output of a first subset of the N storing steps and an output of a second subset of the N storing steps,

wherein a first input of an mth one of the selectings of step (d) is in communication with an output of an m+1th one of the selectings of step (d), and

wherein a second input of the mth one of the selectings of step (d) is in communication with an output of an nth one of the selectings of step (c);

e.) providing the second selection signal to select, M times, one of an output of the selecting of step (d) and an input signal to form the selected signal;

f.) providing the first selection signal to select a subset of the N storing steps,

wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and

g.) providing the second selection signal to select an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword as the output of the pre-selected CRC polynomial keyword.

80. (Previously Presented) The method of claim 79, wherein M is equal to N-1, and

wherein an output of an Nth selecting of step (c) is in communication with the first input of an Mth selecting of step (d).